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DIBL Mitigation Strategies in Gate-all-around Fets for Low Power Performance

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Abstract. The high demand for low-power data processing in AI chips has necessitated the development of high-performance transistors. To suppress the critical drain-induced barrier lowering (DIBL) effect in gate-all-around field-effect transistors (GAAFETs), this paper examines three representative strategies: dual-metal hetero-dielectric (DM-HD) GAAFET architecture, modulation of high-k interfacial layer (IL) thickness, and nanosheet width scaling. While the DM-HD GAAFET architecture applies work-function engineering and hetero-dielectric integration, the latter two strategies focus on parametric or geometrical modulations. DIBL values are further compared across device configurations spanning DM-HD-VA (vacuum-gate), DM-HD-NA (nitride-gate), and parametric variations in high-k IL thickness and nanosheet width. Simulations utilize different physical parameters. The analysis adopts a two-step normalization. The comparison is thereby fair. These normalized data reveal that high-k IL modulation and width scaling yield lower DIBL values than the DM-HD GAAFET architecture. Parametric and geometrical approaches prove more effective in suppressing DIBL. These results are expected to provide guidance on design trade-offs for energy-efficient transistors in AI chips.

Keywords: Drain Induced Barrier Lowering, Gate-all-around, Low power performance

1. Introduction

The mounting computational workloads of artificial intelligence (AI) techniques have led to massive demand for data processing. This mandates energy-efficient processors. Meeting these requirements depends on the continuous refinement of logic transistors, the core component of AI hardware [1, 2]. In recent years, transistor architectures have undergone significant evolution to sustain continuous scaling beyond the 7nm node. Among them, the gate-all-around field-effect transistor (GAAFET) is distinguished by its unique structure and is now crucial for AI chip applications. In particular, its geometry-enabled power efficiency and superior electrostatic control make GAAFET pivotal for AI chip performance enhancement.

The gate-all-around structure provides superior channel control; yet it remains vulnerable to drain-induced barrier lowering (DIBL), a parasitic electrostatic effect that depresses the threshold voltage as the drain voltage increases. Consequently, it contributes to increased subthreshold leakage current, which in turn increases power dissipation in nanoscale devices. Relative to FinFET,

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GAAFETs exhibit attenuated DIBL. Nevertheless, DIBL remains a persistent challenge for achieving high drive current and low subthreshold leakage in aggressively scaled devices.

Prior studies have explored DIBL suppression in GAAFETs through high-k interface layer, work function modulation, and nanosheet scaling [3, 4]. Yet, these approaches introduce trade-offs between DIBL suppression and power consumption. This paper evaluates three representative DIBL mitigation strategies for GAAFETs: the DM-HD GAAFET architecture, modulation of high-k interfacial layer (IL) thickness, and nanosheet width scaling. Through simulation-based analysis and data normalization, relatively effective strategies to suppress DIBL effect are obtained. The results offer practical guidance for the design of low-power GAAFETs in future AI and HPC applications.

2. Device structure and theoretical analysis of DIBL effect

2.1. Gate-all-around FETs structure compared with former FETs

As FinFETs begin to face scaling limitations, GAAFETs have emerged with a gate-all-around structure which provides enhanced scalability compared to FinFETs. As shown in Fig. 1, the GAAFET evolves from the FinFET by replacing the fin (Fig. 1(a)) with a nanosheet (Fig. 1(b)).

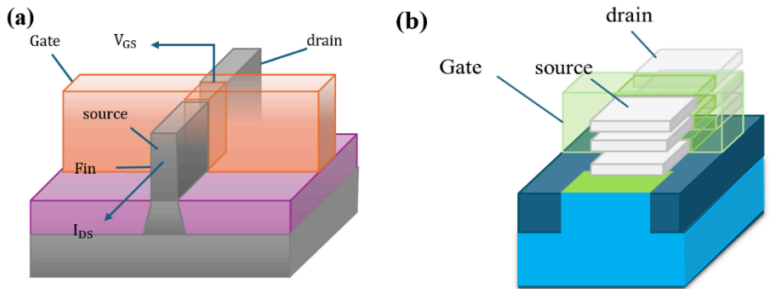


Figure 1. Schematics of (a) FinFET and (b) GAAFET structure

The FinFET, where the gate encloses three surfaces of the fin, enables voltage-controlled current flow across the source-drain path. Unlike FinFET, the surrounding gate of GAAFETs contributes to superior electrostatic control [5]. Moreover, GAAFETs demonstrate remarkably improved controllability owing to their larger gate-contact area and stacking capability, which enhances the switching performance and short-channel effect (SCEs) mitigation [6].

Although continuous scaling offers better electronic characteristics from FinFETs to GAAFETs, DIBL effect still exists and leaves a challenge for transistors' development.

2.2. Mechanism of the DIBL effect

As Moore's Law continues, transistor density on a single IC increase. However, channel scaling leads to undesirable effects, such as SCEs in the device. In short-channel devices, excessive source-drain junction depth or insufficient channel doping can result in DIBL. This arises from undesirable electrostatic interactions between the source and drain.

Essentially, growth and overlap of source and drain depletion regions contribute to DIBL, which causes punch-through between the source and drain. More fundamentally, DIBL arises from the reduction of the source-side barrier beneath the equilibrium level [7].

In GAAFETs, the gate region surrounds the entire channel, and the radial electric field emanating from the gate modulates the channel potential. This electric field provides a clear path for charge carriers to transport from source terminal toward the drain. Moreover, the DIBL phenomenon

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manifests as a negative shift in threshold voltage (V_{th}) of the device under higher drain-to-source voltage (V_{DS}). Owing to the surrounding-gate structure across the channel region, GAAFETs offer superior control over the channel than FinFETs.

2.3. Key performance indicators

Switching ratio (I_{on}/I_{off}): switching ratio can be quantified as state current over off state current, which emphasizes the switching performance of the device. This study evaluates the electric performance of GAAFETs from switching ratio.

DIBL: DIBL is an important sub-threshold performance metric and can be quantified as equation (1)

$$\mathrm{DIBL} = (V_{tlin} - V_{tsat})/(V_{Dsat} - V_{Dlin}) \tag{1}$$

V_{tlin} is the threshold voltage derived from the linear region. By measuring the DIBL value, the severity of the DIBL effect can be assessed. In this research, the DIBL value is used to evaluate the extent of DIBL mitigation [8].

3. Comparative analysis of reported DIBL mitigation strategies

3.1. DM-HD GAAFET architecture

It is important to reduce power dissipation in today's cutting-edge technologies. However, as channel scaling progresses, unexpected SCEs emerge, which hinders higher device performance [5]. To address this issue, Researchers have proposed multiple strategies to mitigate leakage current in GAAFETs. Among these studies, both paper [3] and paper [9] combine GAAFET with the gate material engineering (GME) and hetero-dielectric gate oxide to reduce DIBL in GAAFETs.

Generally, in gate material engineering (GME), the source-adjacent region adopts higher-work-function metals, which increase the threshold voltage and enhance gate control, thereby accelerating source-to-drain charge-carrier transport, whereas the drain-adjacent region adopts lower-work-function metals. These accelerated charged carriers collect at the drain region and increase I_{on}. However, they cause an unexpected increase in tunneling current at the drain and an extra electric field at the interface between channel and drain.

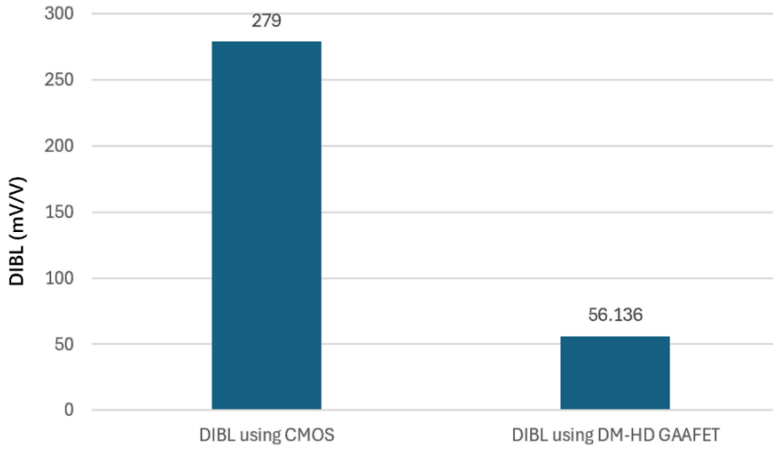


Figure 2. DIBL simulated result of DIBL for CMOS and DM-HD GAAFET

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For the hetero-dielectric technique, a high permittivity (high-k) material is placed on the drain side, which suppresses charge-carrier tunneling and decreases the parasitic field intensity at the channel-drain interface, whereas the low-permittivity material is placed near the source. In 2020, Amit Kumar developed a Verilog-A model for DM-HD GAAFET and applied it to the design of highly efficient logic gates [3]. The DM-HD variant's electrostatic advantages over conventional CMOS are reviewed here. Fig. 2 illustrates that this architecture achieves approximately 80% DIBL mitigation, thereby diminishing power dissipation.

Reference [9] presents a DM-HD-NA GAAFET, in which a high-work-function metal is placed adjacent to the source and a higher-permittivity material is placed near the drain. This design integrates GME and hetero-dielectric techniques. Their research compares DIBL between the vacuum-gate version (DM-HD-VA GAAFET) and the nitride-gate version (DM-HD-NA GAAFET). In 2019, Kumar et al. studied the suppression of DIBL using a DM-HD-NA GAAFET. Their study summarized the comparison between the vacuum-dielectric and nitride-dielectric variants [9]. Fig. 3 shows that the NA variant exhibits lower DIBL than the VA variant, indicating superior DIBL immunity. These stems from weakened interfacial field intensity at the oxide-channel boundary in the NA variant. Notably, the DIBL value of the VA variant was previously calculated in [10].

Furthermore, from the simulated field profiles of DM-HD-VA GAAFET and DM-HD-NA GAAFET in paper [9] when V_{GS} is 0V to 1V, DM-HD-VA GAAFET exhibits a more pronounced DIBL because it has intensified electric field at the oxide channel interface. In the nitride-dielectric design, however, the DIBL is alleviated owing to its lower electric field at the oxide channel interface conferred by the inserted high permittivity material layer. The interfacial field can be reduced by a factor of $\varepsilon/\varepsilon_0$, where ε denotes the permittivity of nitride.

Therefore, it is demonstrated that DIBL in GAAFET can be effectively mitigated by combining GME and hetero-dielectric technologies. It helps mitigate charge carriers tunneling and reduce unexpected electric field at the channel drain interface. This DM-HD-NA GAAFET achieves effective DIBL suppression, providing a valuable reference for future research.

Moreover, the DIBL value in 3.1 requires further processing due to its relatively long channel length (30nm) and nanowire structure in this simulation. Therefore, normalization and data processing will be implemented in 3.4 for fair comparison.

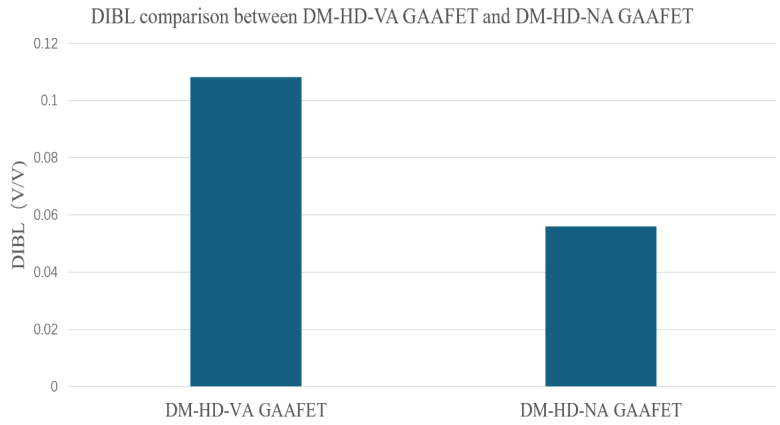


Figure 3. DIBL simulated result of the vacuum-dielectric variant and the nitride variant

3.2. Modulation of high-k IL thickness

Scaling down the oxide thickness (T_{ox}) strengthens the electrostatic coupling between the gate electrode and the channel, which can mitigate SCEs. However, aggressive T_{ox} scaling has arisen

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some problems about OFF current because of gate tunneling. Reference [5], [8] and [9] all indicate that utilizing high-k materials can reduce leakage current. Therefore, a high-k gate dielectric was adopted starting at 45 nm node to overcome this issue. Nevertheless, to reduce thermal exposure of heat-sensitive metal gates and high-k dielectrics, a gate-last scheme is necessitated. During this process, the high-k interfacial layer (IL) spontaneously forms between the gate and the inner spacer. The presence of this IL modulates electrostatic behavior, with device parameters demonstrating pronounced sensitivity to its thickness variation.

In 2020, Donghyun Ryu et al. investigated the high-k IL thickness engineering in a 5-nm-node nanosheet FET (NSFET), with the IL localized at the interface between the gate stack and the inner sidewall spacer [4]. This paper summarizes their electrostatic characteristics from that research. Specifically, Fig.4 (a) depicts DIBL as a function of T_{hk}, while Fig.4 (b) shows I_{on}/I_{off} versus T_{hk}. As T_{hk} increases, DIBL deterioration is observed, demonstrating reduced electrostatic gate control.

Moreover, I_{on}/I_{off} in Fig.4 (b) exhibits an increasing trend with increasing T_{hk}, highlighting the trade-off between electrostatic control and power efficiency.

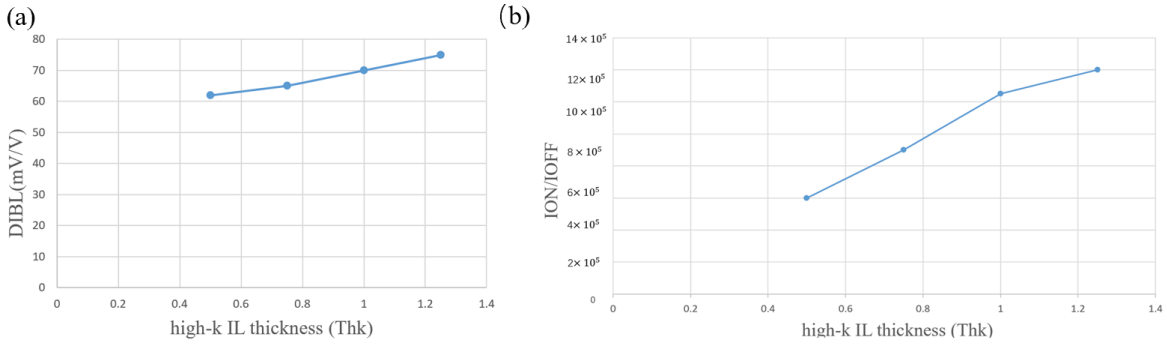


Figure 4. Plot of (a) DIBL according to T_{hk} (nm) and (b) I_{on}/I_{off} versus T_{hk}

3.3. Nanosheet width scaling

Another approach to mitigate DIBL effect is to improve gate control over the channel. Multi-gate devices, such as GAAFETs, provide superior potential control over the device to FinFETs. However, nanowire-based GAAFETs suffer from limited drive current due to their narrow effective widths. Nanosheet GAAFETs (GAA NSFET) offer enhanced electrostatic control and effective mitigation of SCEs [8]. Nevertheless, the TCAD simulation proposed by paper [11] demonstrates that the SCE superiority of the NSFET is valid only for narrow NSFET width (w_{si} , noted that N_w is used in this paper for nanosheet width). Once $w_{si} > \sim 4 \times t_{si} = 20$nm, NSFET will miss this SCE superiority. Therefore, this study uses NSFET whose N_w is 10 nm, sheet thickness (N_T) is 5 nm, and gate length (L_G) is 16 nm in the simulation.

When nanosheets are incorporated with small widths and thickness, the DIBL will be mitigated, thereby showing that DIBL can be modified by changing the value of width and thickness. In 2021, N. Aruna Kumari investigated DC performance variations of 3D NSFET under different geometrical configurations [8]. This paper summarizes the relationship between DIBL and N_w and between I_{on}/I_{off} and N_w , as shown in Fig. 5 and 6. Fig. 5 demonstrates that as N_w increases, DIBL will increase as well, offering direct evidence of the influence of changing N_w on DIBL.

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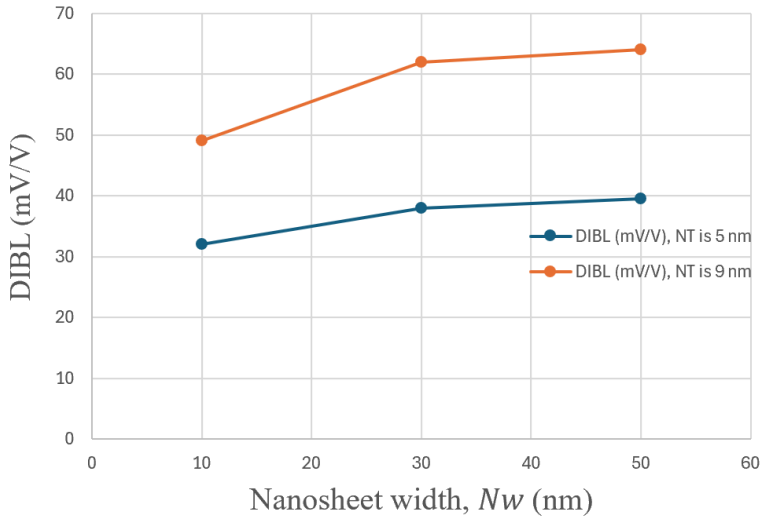


Figure 5. DIBL (mV/V) versus nanosheet width (nm)

Moreover, the DIBL value is calculated by the value of V_{th} which shows decreasing trend as the N_w increases. V_{th} drops dramatically by 5.3% (5 nm N_{T}) and 8% (9 nm N_{T}) when the nanosheet width changes from 10 nm to 50 nm. This V_{th} roll off correlates with the enhanced DIBL effect, further validating that the deterioration of SCEs.

Other parameters from this simulation also prove that as N_w increases, DIBL Effect becomes severe. Fig. 6 shows the switching ratio (I_{on}/I_{off}) decreases as N_w increases. Furthermore, as width increases, the switching ratio drops by 71% and 94% for 5 nm and 9 nm thickness, respectively [8].

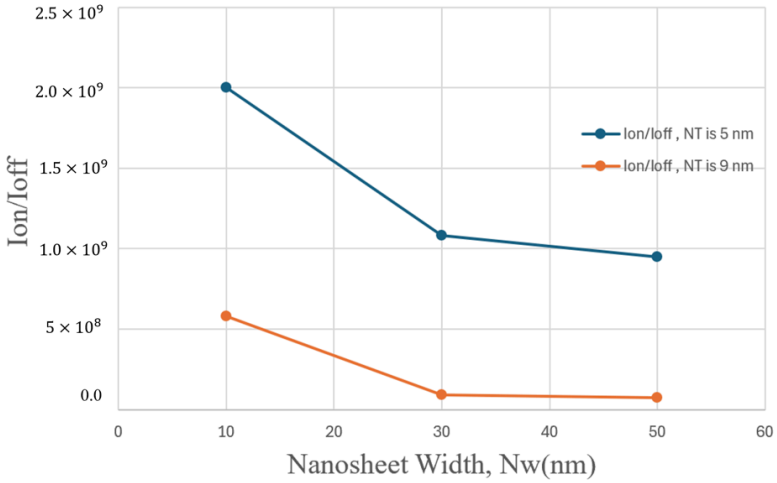


Figure 6. I_{on}/I_{off} versus nanosheet width (nm)

3.4. Data processing and comparable analysis

Table 1 compares DIBL values extracted from Sections 3.1, 3.2 and 3.3, and the approximate values are employed because data are obtained from plots.

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Table 1. DIBL for sections 3.1, 3.2 and 3.3

Strategies in Sections 3.1, 3.2 and 3.3	Channel length (L_G) (nm)	DIBL (mV/V)
DM-HD GAAFET	30	56.136
Modulation of high-k IL thickness	12	60~75
Nanosheet Width Scaling	16 [8]	30~65

However, these simulation conditions are different. Diameter of the nanowire in Section 3.1 is 20nm, DIBL in Section 3.2 has great variation for different T_{hk} from 0.5 nm to 1.25 nm, and DIBL in Section 3.3 changes from approximately 32 to 38 mV/V at a sheet thickness of 5 nm. With the aim to find out the most effective method to mitigate DIBL, harmonizing device parameters is the first step.

To address the DIBL value of Section 3.1, paper [12] provides DIBL values of nanowire and nanosheet under identical simulation situations, which offers a quantitative relationship between their DIBL values. Based on these data, the factor of 0.65 is derived between the nanosheet and the nanowire ($\frac{153.8\ \mathrm{mV/V}}{238.5\ \mathrm{mV/V}} \approx 0.65$). $DIBL_{nanosheet(3.1)} \approx DIBL_{nanowire(3.1)}$ *0.65 $\approx$ 56.136 * 065 $\approx$ 36.4884.

Furthermore, DIBL values should be normalized to the same channel length. Equation (2) offers a relationship between DIBL and channel length [13].

$$\theta_{th}(L) = [\exp(-\mathrm{L}/2\mathrm{l}_t) + 2\exp(-\mathrm{L}/\mathrm{l}_t)] \tag{2}$$

Where $\theta_{th}(L)$ is the short channel effect coefficient. $DIBL_{normalized} = \frac{DIBL}{\theta_{th}(L)}$.

Taking 8nm as the l_t , the calculated results are in Table 2, $DIBL_{normalized(3.2)} < DIBL_{normalized(3.3)} < DIBL_{normalized(3.1)}$. Notably, the $DIBL_{normalized(3.1)}$ is much larger than $DIBL_{normalized(3.2)}$ and $DIBL_{normalized(3.3)}$, which demonstrates that modulation of high-k IL thickness and nanosheet width scaling are more effective than DM-HD GAAFET architecture. However, it is hard to distinguish which method stands out due to the similarity of DIBL values between Sections 3.2 and 3.3. Since Sections 3.2 and 3.3 involve parametric and geometrical modulations, it can be concluded that parametric and geometrical modulations are the most effective strategies to suppress the DIBL effect in GAAFETs.

Table 2. Normalized data for sections 3.1-3.3

Normalization of channel length	Channel length (L_G) (nm)	channel width(nm)	$\theta_{th}(L)$	$DIBL_{normalized}$
DM-HD GAAFET	30	/	0.2004	182.09
Modulation of high-k IL thickness	12	25	0.9186	73.48
Nanosheet Width Scaling	16	25	0.6386	74.39

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4. Future outlook

GAAFET's distinctive gate-all-around structure offers inherent advantages in channel control and superior electrical performance. As hetero-dielectric integration, nanosheet width scaling, and high-k IL engineering mature, drive-current capability is expected to improve. Reference [14] reports a novel approach, ultra-low-temperature operation, that improves GAAFET electrostatics and markedly suppresses DIBL. The outlook suggests that GAAFET technology will incorporate multiple enhanced strategies and enable high-performance logic applications.

AI inference and training workloads demand higher computational throughput, faster response times, and expanded memory bandwidth. These demands spur different transistor-level strategies to enhance electrostatic control. For instance, nanosheet width scaling combined with an appropriate number of stacked nanosheets facilitates optimal area-performance-power trade-offs [15]. Therefore, this flexibility will offer designers greater freedom to tailor GAAFET-based AI chips for various application requirements.

5. Conclusion

In this paper, three representative DIBL mitigation strategies in GAAFET are compared: DM-HD GAAFET architecture, modulation of high-k IL thickness, and nanosheet width scaling. Simulated results of DIBL values from previous research and data processing are employed to enable comparable analysis. Considering the inconvenience of comparing, it is more easily analyzed after normalization. Therefore, two steps of normalization are required. The first step is to normalize DIBL in 3.1 from a nanowire structure into a nanosheet structure. Second, harmonize DIBL values across different channel lengths. Results from this analysis emphasize that modulation of high-k IL thickness and nanosheet width scaling are more effective methods to suppress DIBL. Moreover, the DIBL values achieved by these two strategies are comparable, demonstrating that parametric and geometrical adjustments are generally more effective than the DM-HD architecture for DIBL suppression in GAAFETs.

Therefore, the evaluated strategies in this study offer superior DIBL mitigation with a relatively low power-consumption trade-off. This quantitative comparison establishes a parameter tradeoff landscape in GAAFET. It indicates distinct performance for each approach, thereby supporting designers to account for diverse AI chips requirements.

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