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Comparative DC and AC Response of Short-Channel NMOS Test Structures Using the MVS Model and a 65-nm Foundry Model

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Abstract. This work presents a compact-model-level comparison between the MIT virtual-source (MVS) model and a 65-nm foundry model for short-channel NMOS devices and simple load-dependent test circuits. A short-channel device schematic based on the MVS concept is first used to establish the physical picture of virtual-source-controlled transport. Two single-transistor test structures are then evaluated: a reference branch without a source resistor and a branch with a source load. Using the provided DC voltage, DC current, and AC frequency-response characteristics, the two models are compared in terms of output-voltage transition, current build-up, and bandwidth roll-off behavior. The results show that both models capture the qualitative impact of loading, but they differ noticeably in the transition location of V_{DC}, in the low-to-intermediate-bias rise of I_{DC}, and in the onset of AC roll-off. Under the present test conditions, the MVS model exhibits earlier DC transition, faster current establishment, and a later AC roll-off than the 65-nm foundry model. These observations indicate that a virtual-source-based compact description is not merely an alternative fitting form, but a physically meaningful modeling layer that can influence circuit-level predictions even in very simple transistor test structures.

Keywords: MVS model, short-channel MOSFET, compact modeling, DC characteristics, AC response

1. Introduction

Compact modeling for aggressively scaled MOSFETs must reconcile two competing requirements: circuit-level efficiency and physically meaningful representation of short-channel transport. Among the best-known physics-inspired compact approaches, the MIT virtual-source (MVS) model introduced a compact current–voltage formulation for short-channel MOSFETs that remains continuous across operation regions while retaining a small set of physically interpretable parameters [1]. The framework was later extended to self-consistent current and charge formulations that cover transport regimes from ballistic to drift–diffusion velocity saturation [2]. Lundstrom and Antoniadis further clarified how the virtual-source viewpoint connects compact-model parameters to nanoscale device physics, making the model especially relevant when source-end injection and quasi-ballistic transport are non-negligible [3].

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This line of work remains relevant because the scaling problem has not disappeared; rather, it has broadened. Recent studies on ultimately scaled transistors, short-channel effects in nonconventional devices, and new compact-model directions all indicate that physically grounded compact descriptions remain important even when new fitting strategies are introduced [4-6]. In parallel, short-channel behavior continues to affect practical readout and buffer circuits, including source-follower-related structures used in image-sensor front ends and low-voltage analog interfaces [7-11]. These developments suggest that the question is no longer whether short-channel physics matters, but how strongly a given compact-model layer propagates into observable circuit-level behavior.

In this context, the present paper studies a deliberately simple but instructive case. Using the supplied figures, a foundry-style 65-nm transistor model and the MVS model are compared at two levels: device interpretation and single-transistor circuit response. Rather than pursuing a large benchmark set or complex circuit demonstrations, the study focuses on one short-channel device schematic, two test structures, and six response plots. This restricted setup is intentional because it allows the effect of the compact model itself to remain visible, instead of being obscured by circuit complexity.

The main contributions of this work are threefold. First, the MVS short-channel device picture is linked to a concrete test methodology using the supplied device schematic and two drain-readout transistor test circuits. Second, the two models are compared consistently in terms of V_{DC}, I_{DC}, and V_{AC} responses under identical structural changes. Third, the observed differences are interpreted from a compact-model perspective, showing that the MVS model changes not only device-level intuition but also the predicted behavior of simple load-dependent transistor stages.

2. Device picture and test structures

2.1. Short-channel device picture under the MVS framework

Figure 1 illustrates the short-channel transistor picture used throughout this work. The key feature is the explicit identification of the virtual-source region near the source-side channel barrier. In the MVS framework, current establishment is governed less by a long-channel gradual-channel perspective and more by the source-end injection condition, together with a compact representation of short-channel transport and velocity limitation. This viewpoint is particularly useful when the gate length is sufficiently short that a purely long-channel drift-based intuition becomes inadequate.

This physical interpretation remains relevant in recent literature. Reviews of ultimately scaled transistors emphasize that channel control, source injection, and transport nonidealities become increasingly coupled as the physical length scale is reduced [4]. Similar motivations appear in recent short-channel compact-model work, including design-oriented single-piece models, data-assisted MOSFET I–V modeling, and hybrid formulations for quasi-ballistic nanotransistors [12, 13]. In addition, previous study explicitly revisits extremely scaled transistor modeling through the virtual-source framework, which further motivates including the MVS perspective in a modern comparison study [14].

Figure 1 provides the physical basis for the subsequent model comparison. It serves as a compact physical interpretation of short-channel transport, where the source-end virtual-source region governs the current establishment process.

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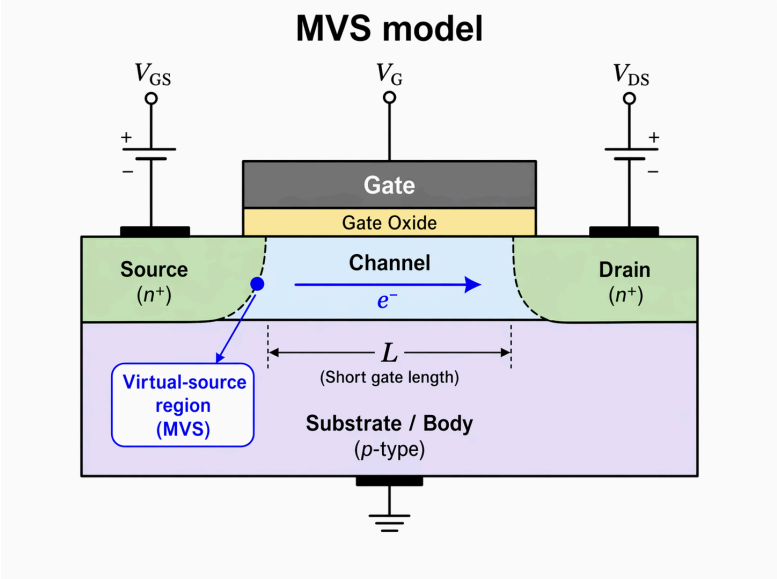

Figure 1. Short-channel NMOS device picture used in this work. The virtual-source region is highlighted near the source-side barrier, and the schematic emphasizes the short gate length and source-end injection path central to the MVS interpretation

2.2. Single-transistor test structures

Figure 2 shows the two test circuits used in this work. For scientific consistency, they are referred to here as single-transistor drain-readout test structures, because in the final schematic the output node V_{out} is taken at the drain-side node. Structure (a) uses a direct source-to-ground connection, while structure (b) introduces a source resistor R_S. This pair provides a compact way to probe how the model responds to a basic structural change in source-side loading.

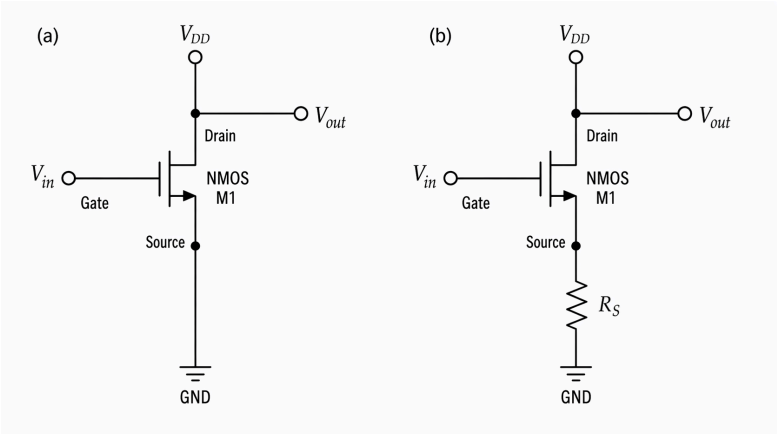

Figure 2. Single-transistor drain-readout test structures used for model comparison: (a) branch without a source resistor and (b) branch with a source load R_S

Although the circuits are intentionally simple, the structural question they pose is meaningful. Load conditions and source-side degeneration affect node-voltage establishment, current drive, and AC roll-off in short-channel transistors and in transistor-based readout stages [15]. Thus, even though the present study is not a full pixel-chain or analog-front-end design paper, the chosen structures remain relevant as reduced test vehicles.

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The two structures differ only in the source-side loading path. This controlled difference allows the change in compact-model response to be attributed to the source-load perturbation rather than to circuit-topology variation.

3. DC output-voltage characteristics

3.1. Foundry-model response

Figure 3 compares the drain-readout V_{DC} response of the two structures using the 65-nm foundry model. In the low-V_D region, both curves remain at a high output plateau, followed by a gradual transition to a lower-voltage regime as V_D increases. The branch with source loading (1R) preserves a higher V_{DC} over most of the sweep and exhibits a smoother and more right-shifted transition than the branch without source loading (0R). Within the scope of the present plots, this indicates that the source resistor redistributes the node bias in a manner that delays output collapse.

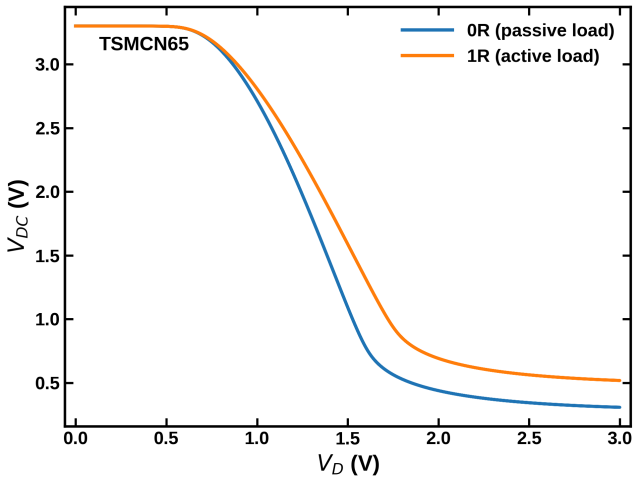

Figure 3. Comparison of V_{DC} versus V_D for the 65-nm foundry model. The 0R and 1R branches show different transition positions and different output-voltage retention with increasing V_D

The overall transition is smooth, without abrupt numerical artifacts, which is consistent with the role of foundry-ready models in robust circuit simulation. Such models are typically optimized not only for device fitting but also for numerical continuity and design-environment stability across broad operating regions [1, 3, 5, 6].

Figure 3 shows that source loading shifts the output-voltage transition to higher V_D and maintains a larger output level over much of the sweep in the foundry-model case.

3.2. MVS-model response

Figure 4 shows the corresponding V_{DC} characteristics obtained from the MVS model. The most apparent difference relative to Figure 3 is that the transition occurs earlier and more abruptly. The 0R branch drops rapidly over a narrower V_D interval, and the 1R branch, although still maintaining a higher output level than 0R, also transitions at lower V_D than in the foundry-model case.

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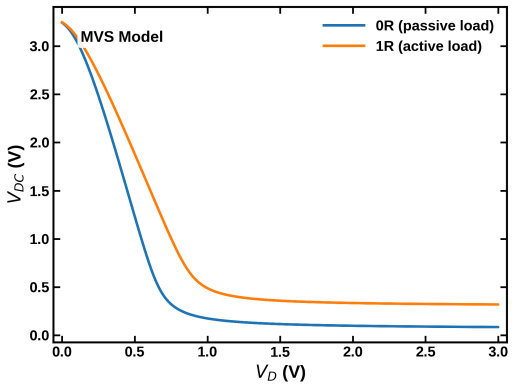

Figure 4. Comparison of V_{DC} versus V_D for the MVS model. The transition occurs earlier and more sharply than in the foundry-model case

This earlier transition is consistent with a compact model that is more sensitive to source-side injection and short-channel transport control. Because the MVS formulation is built around a virtual-source transport picture, its effective transition behavior can become more concentrated in bias space than in a more heavily calibrated foundry model [1-3, 9, 12, 13].

Figure 4 indicates that the MVS model predicts a stronger sensitivity of the output-voltage transition to terminal bias, especially for the branch without source loading.

4. DC current characteristics

4.1. Foundry-model response

Figure 5 presents the semilog I_{DC}–V_D characteristics for the foundry model. At very low bias, the 0R and 1R branches are close to each other. As V_D increases, the current rises over multiple decades and the 0R branch becomes moderately larger than the 1R branch before both eventually approach a high-current regime. This behavior suggests that, under the foundry model, source loading suppresses current drive primarily in the intermediate and high-bias regions, while its effect on the earliest current build-up is comparatively modest.

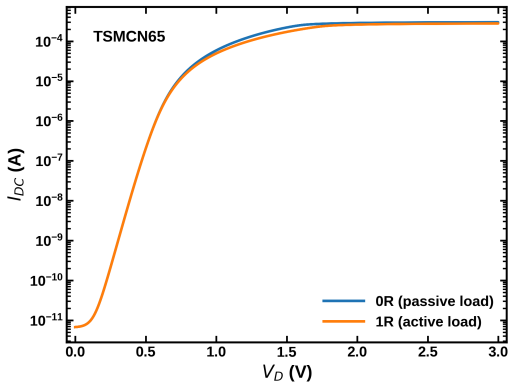

Figure 5. Semilog comparison of I_{DC} versus V_D for the 65-nm foundry model. The current difference between the 0R and 1R branches becomes visible mainly in the intermediate and high- bias regions

Such behavior is compatible with compact models that are tuned to maintain good global agreement over the operating space rather than to explicitly expose a single physical short-channel

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mechanism at each bias point [1, 3, 6].

Figure 5 shows that the foundry model captures the expected current suppression due to source loading, but the low-bias onset remains very similar for the two branches.

4.2. MVS-model response

Figure 6 shows that the MVS model yields a different current-evolution profile. The current rises more rapidly from low bias, and the separation between 0R and 1R is more pronounced over the low-to-intermediate-V_D range. In particular, the 0R branch reaches the higher-current region earlier than in the foundry-model case, while the 1R branch remains visibly suppressed by the source load.

This observation reinforces the interpretation already suggested by the V_{DC} results: the MVS model changes not only the output-voltage transition point, but also the way conduction builds up as the terminal bias increases. Since the original MVS model was designed precisely to describe short-channel MOSFET I–V behavior with physically meaningful parameters, stronger low-to-medium bias sensitivity is not unexpected [1, 2].

Figure 6 suggests that the MVS formulation is more sensitive to source-side loading during the conduction-establishment process.

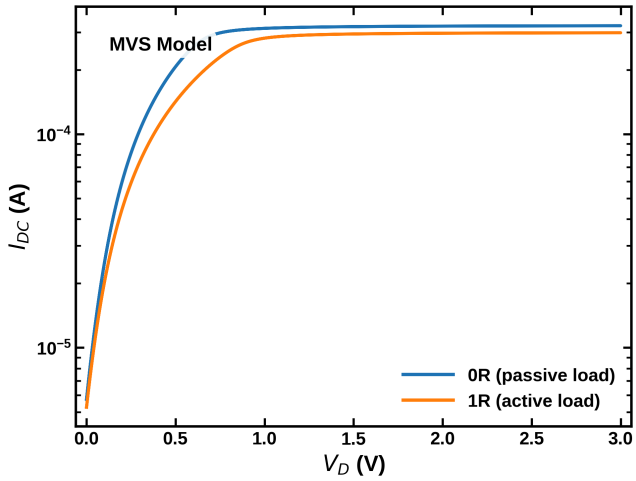

Figure 6. Semilog comparison of I_{DC} versus V_D for the MVS model. The 0R and 1R branches separate earlier, and the current build-up begins more rapidly than in the foundry-model case

5. AC frequency response

5.1. Foundry-model response

Figure 7 compares the AC magnitude response predicted by the foundry model. Both branches show a flat low-frequency region followed by a sharp roll-off at high frequency. The 0R branch begins from a higher low-frequency magnitude, while the 1R branch shows a lower low-frequency level but retains a higher residual magnitude after roll-off. In other words, introducing the source load trades low-frequency amplitude for a more elevated high-frequency tail in the present test structure.

This kind of tradeoff is familiar in transistor-based readout chains and source-follower-related front ends, where static biasing, load conditions, and parasitic redistribution jointly shape both low-frequency operation and high-frequency poles [7-11, 14].

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Figure 7 indicates that source loading modifies not only the low-frequency magnitude but also the high-frequency asymptotic behavior in the foundry-model case.

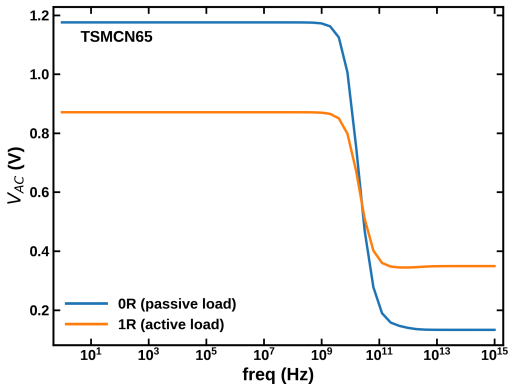

Figure 7. Comparison of V_{AC} magnitude versus frequency for the 65-nm foundry model. The 0R branch shows a higher low-frequency level, while the 1R branch retains a larger post-roll-off tail

5.2. MVS-model response

The MVS AC response in Figure 8 preserves the same qualitative branch ordering but shifts the dominant roll-off to higher frequency. Compared with Figure 7, the onset of attenuation is clearly delayed. At the same time, the low-frequency separation between 0R and 1R remains evident, with 0R exhibiting the larger low-frequency magnitude. As the frequency increases further, the two branches converge toward similar asymptotic levels.

Taken together with the DC plots, Figure 8 suggests a consistent trend: under the present parameterization, the MVS model predicts a device that is both more responsive in current establishment and more resistant to high-frequency attenuation. This does not imply that the MVS model is universally better than the foundry model; rather, it indicates that the two model layers encode different assumptions and priorities [1-3, 12, 13, 15].

Figure 8 shows that the MVS model predicts a later frequency roll-off than the foundry model under the same structural perturbation.

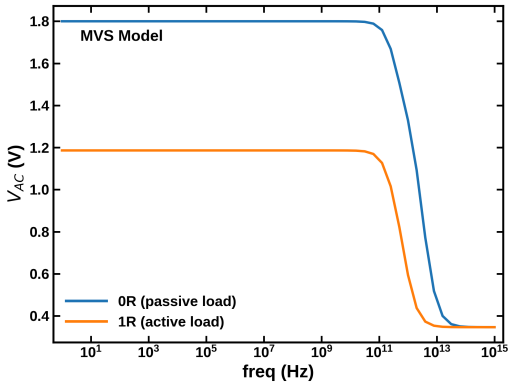

Figure 8. Comparison of V_{AC} magnitude versus frequency for the MVS model. The dominant roll-off moves to higher frequency, and the two branches converge only after the high-frequency transition

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6. Discussion

Three observations emerge consistently from Figs. 3–8. First, both models capture the direction of the loading effect. Introducing the source resistor changes V_{DC}, I_{DC}, and V_{AC} in all cases. Therefore, even in a minimal one-transistor test environment, load conditions are sufficient to expose measurable model-dependent behavior.

Second, the MVS model is clearly more sensitive to short-channel transport reconfiguration under the same structural perturbation. Relative to the foundry model, it predicts earlier V_{DC} transition, faster I_{DC} build-up, and later AC roll-off. This combination suggests a more aggressive short-channel response, consistent with the virtual-source view of current establishment [1-3].

Third, the comparison supports a broader modeling point. A physics-grounded compact model is not merely a replacement for table fitting. Even when evaluated through simple test circuits, it changes the predicted coupling between bias, output-node formation, and bandwidth. This is why recent work continues to pursue physically structured compact models, design-oriented short-channel formulations, and hybrid physics/ML approaches rather than relying solely on black-box fitting [6, 9, 12, 13].

7. Conclusion

A comparative compact-model study of short-channel NMOS device behavior and simple drain-readout test circuits has been presented using a 65-nm foundry model and the MVS model. Based on the supplied device schematic and six response plots, the analysis shows that both models reproduce the qualitative impact of source-side loading, but they differ substantially in output-voltage transition, current build-up, and AC roll-off location. Under the present test conditions, the MVS model exhibits an earlier DC transition, a faster rise in drain current, and a later frequency roll-off than the foundry model. These results support the view that virtual-source-based compact modeling remains valuable not only for device interpretation, but also for circuit-level reasoning in short-channel transistor studies.

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