Proceedings of the 4th International Conference on Applied Physics and Mathematical Modeling
DOI: 10.54254/2753-8818/2026.34200

TCAD-Based Investigation of Gate Oxide Thickness Effects on SOI- MOSFETs

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Abstract. Gate-oxide thickness is a first-order design variable that controls electrostatic coupling, threshold behavior, and leakage in scaled field-effect transistors. This paper presents a compact Silvaco TCAD study of a silicon MOSFET in which the oxide thickness tox is swept from 1 to 5 nm while the drain bias is fixed at VD = 0.05 V. The simulation flow builds the device structure, defines the mesh and regions, assigns material/doping parameters, solves the bias sweep, and extracts transfer characteristics, threshold voltage, and subthreshold swing. The simulated ID-VG curves show a systematic positive shift with increasing tox, indicating weakened gate control. Using the maximum-slope definition of SS and a constant-current threshold criterion of ID = 1 × 10−7 A, the extracted SS increases from 70.57 to 91.31 mV/dec, while Vth increases from 0.029 to 0.517 V as tox increases from 1 to 5 nm. These results provide a clear TCAD-based visualization of the trade-off between gate dielectric scaling, switching efficiency, and threshold-voltage engineering.

Keywords: MOSFET, gate oxide thickness, threshold voltage, subthreshold swing, constant-current method, device simulation

1. Introduction

Gate-stack engineering remains central to CMOS device scaling because the gate dielectric determines how efficiently the gate potential modulates the channel charge. In classical MOSFET theory, a thinner oxide increases the gate capacitance and strengthens electrostatic control, while a thicker oxide reduces the gate field and shifts the transfer curve toward higher gate voltage [1, 2]. Although modern logic devices increasingly employ high-k dielectrics, metal gates, FinFETs, nanosheets, and gate-all-around architectures, the physical role of equivalent oxide thickness remains the same: it sets the coupling between gate bias and channel potential.

Technology computer-aided design (TCAD) is widely used to evaluate process and device options before fabrication. Silvaco TCAD provides a device-simulation environment in which process-defined structures, mesh settings, material parameters, doping distributions, physical models, bias sweeps, and output extraction can be organized into a reproducible workflow [3-5]. Such a workflow is valuable for early-stage design because it separates device-physics trends from experimental variability and enables rapid parameter sweeps.

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Recent roadmap discussions emphasize that transistor scaling is no longer governed by a single geometrical parameter. Gate-stack thickness, interface quality, device geometry, and metrology uncertainty must be considered together when evaluating future logic technologies [6, 7]. Among these quantities, tox is particularly important because it directly affects threshold voltage, subthreshold swing, and the on/off current ratio. Therefore, even a simplified MOSFET TCAD study can provide useful insight into the electrostatic origin of switching behavior.

This work focuses on a controlled tox sweep in a silicon MOSFET. The objective is not to propose a new device architecture, but to establish a clear simulation-based relationship between oxide thickness and extracted device metrics. The main contributions are as follows. First, a concise Silvaco simulation workflow is organized for structure generation, mesh definition, physical-model selection, bias solution, and parameter extraction. Second, transfer curves are generated for tox = 1, 2, 3, 4, and 5 nm. Third, SS is extracted from the inverse maximum slope of log10(ID) versus VG, while Vth is extracted by the constant-current method. Finally, the extracted trends are interpreted in terms of electrostatic gate control and threshold-voltage shift.

2. Simulation methodology

2.1. TCAD workflow

The simulation procedure is summarized in Fig. 1. The device target and parameter space are first defined, including geometry, material system, and electrical metrics. The structure is then built using the Silvaco process/device environment, followed by mesh and region definition. Material parameters, doping profiles, and contact properties are assigned before the physical models and numerical solver settings are activated. Finally, the bias sweep is performed and the resulting I_D-V_G data are post-processed to extract V_{th}, SS, I_{on}, and I_{off}.

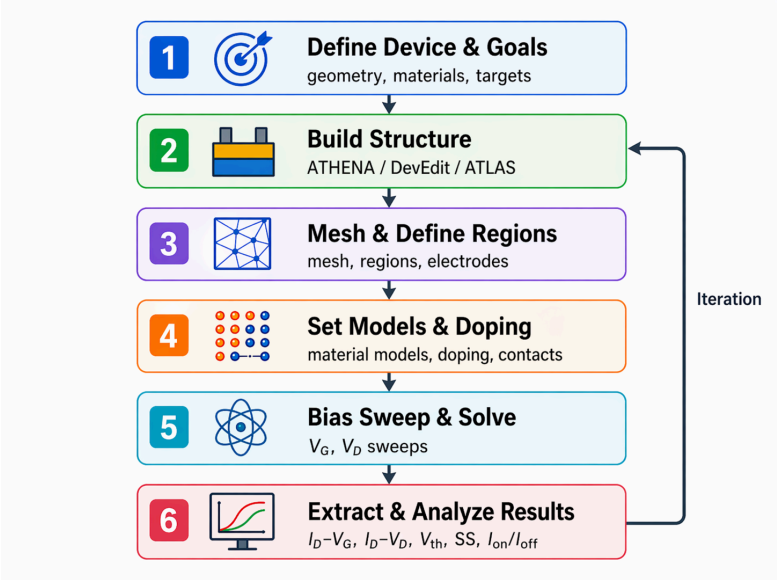

Figure 1. Simplified Silvaco TCAD simulation flow used in this work. The workflow starts from device definition and ends with electrical-parameter extraction. The feedback loop indicates that geometry, models, and doping settings can be iteratively refined

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2.2. Device structure and doping distribution

Fig. 2 shows the simulated device cross-section and doping-concentration distribution. The source/drain regions are heavily doped, while the channel region is controlled by the gate stack. The structure provides a representative MOSFET platform for studying how oxide thickness modifies the gate-to-channel coupling. Since the purpose of this work is to isolate the role of t_{ox}, all other device parameters and bias conditions are kept fixed during the sweep.

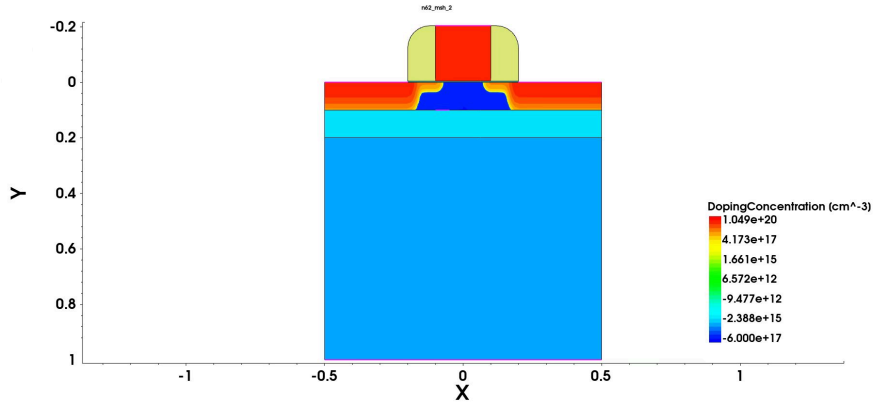

Figure 2. Simulated MOSFET structure and doping-concentration distribution. The color scale represents doping concentration in cm−3, and the plotted cross-section provides the basis for the tox-dependent electrical simulations

2.3. Parameter sweep and extraction definitions

The gate oxide thickness is swept from 1 to 5 nm. For each value, the transfer curve is simulated at V_D = 0.05 V. The subthreshold swing is extracted from the steepest subthreshold region according to:

$$SS = [dlog10(\mathbf{I_D})/d\mathbf{V_G}]^{-}1 \tag{1}$$

where SS is reported in mV/dec. This definition captures the minimum gate-voltage increment required to increase the drain current by one decade. The threshold voltage is extracted using the constant-current method:

$$\mathbf{V_{th}} = \mathbf{V_G} / \mathbf{I_D} = \mathbf{I_{crit}} \tag{2}$$

where the threshold current criterion is $I_{crit} = 1 \times 10^{-7}$ A. Threshold extraction can vary depending on the selected definition and device technology; therefore, the extraction criterion is explicitly stated for reproducibility [8, 9].

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3. Results and discussion

3.1. Transfer characteristics under oxide-thickness scaling

Fig. 3 shows the simulated transfer characteristics for t_{ox} values from 1 to 5 nm. The curves exhibit a clear monotonic shift as t_{ox} increases. The 1 nm oxide case turns on at the lowest gate voltage and reaches a higher current at a given V_G in the subthreshold-to-transition regime. By contrast, the 5 nm oxide case shows delayed turn-on and a larger threshold voltage. This behavior is consistent with the reduced gate capacitance and weaker electrostatic control caused by increasing oxide thickness.

The high-current plateau remains within the same order of magnitude for all cases, indicating that the main impact of oxide scaling in this bias condition is the horizontal shift and subthreshold degradation rather than a drastic change in the final on-state level. In a practical design setting, this implies that t_{ox} selection must balance low-voltage turn-on, leakage suppression, gate reliability, and process feasibility. Similar electrostatic trade-offs are also reported in recent TCAD studies of advanced FET structures and dielectric-engineered devices [10-13].

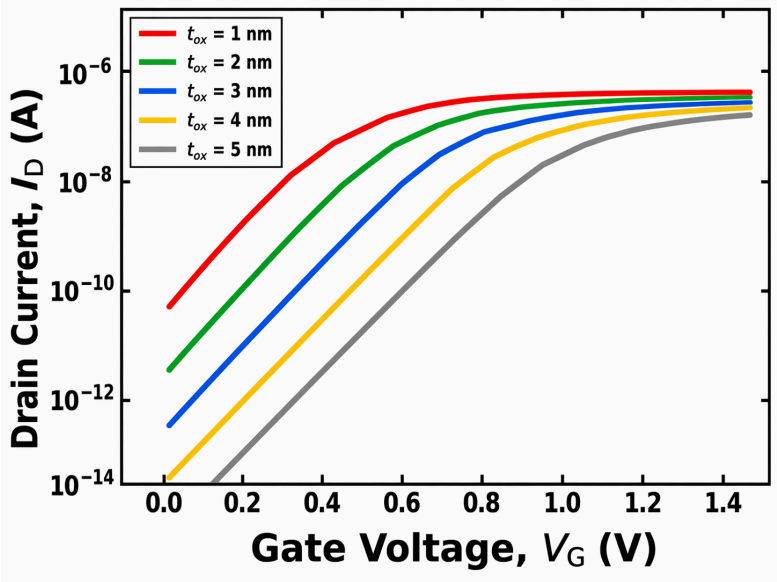

Figure 3. Simulated transfer characteristics at V_D = 0.05 V for tox = 1, 2, 3, 4, and 5 nm. Thinner oxide provides stronger gate control and shifts the transfer curve toward lower gate voltage

3.2. Threshold voltage extracted by constant-current method

Fig. 4 plots the extracted V_{th} as a function of t_{ox}. The threshold voltage increases almost linearly from 0.029 V at t_{ox} = 1 nm to 0.517 V at t_{ox} = 5 nm. The extraction uses $I_D = 1 \times 10^{-7}$ A as the constant-current criterion. Because the transfer curves are horizontally shifted by oxide scaling, the gate voltage required to reach the same drain current increases with t_{ox}. This result directly reflects the reduction in gate capacitance and the weaker inversion control of thicker oxide.

The threshold-voltage trend is important for low-power design. A smaller V_{th} enables lower-voltage operation but can increase standby leakage, while a larger V_{th} suppresses leakage but requires a higher gate overdrive. Recent studies on FD-SOI, high-k dielectric stacks, and emerging transistor channels show that threshold extraction and dielectric selection remain key concerns even beyond conventional planar MOSFETs [14-18].

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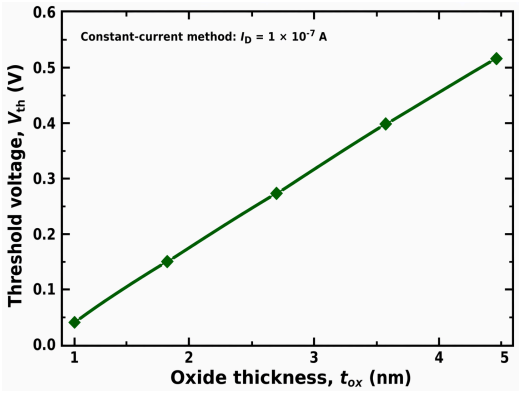

Figure 4. Threshold voltage extracted as a function of oxide thickness using the constant-current method with ID = 1 × 10−7 A. Vth increases from 0.029 to 0.517 V as tox increases from 1 to 5 nm

3.3. Subthreshold swing and gate-control degradation

Fig. 5 shows the extracted SS versus t_{ox}. SS increases from 70.57 mV/dec at t_{ox} = 1 nm to 91.31 mV/dec at t_{ox} = 5 nm. This monotonic degradation indicates that the gate voltage becomes less efficient in modulating the channel current as the oxide is thickened. In an ideal long-channel MOSFET at room temperature, SS approaches the thermal limit of approximately 60 mV/dec. The values obtained here remain above this limit, which is expected because practical structures include finite electrostatic coupling, depletion capacitance, and nonideal numerical/device factors.

The simultaneous increase of V_{th} and SS provides a compact picture of the t_{ox} trade-off. A thinner oxide improves switching steepness and reduces the gate voltage needed to reach a target current. However, extremely thin dielectrics may raise concerns about direct tunneling, reliability, and process variation. Conversely, thicker oxide improves dielectric robustness but weakens electrostatic control. This trade-off motivates continued interest in high-k materials and carefully optimized gate stacks, which can reduce equivalent oxide thickness without physically using an ultra-thin SiO_2 layer [19-23].

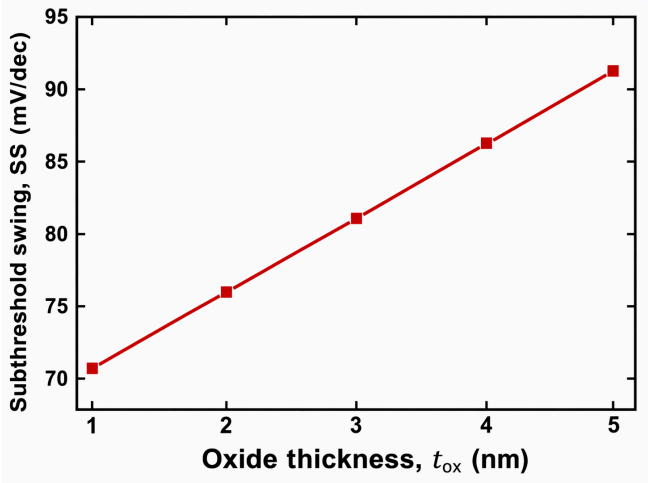

Figure 5. Extracted subthreshold swing as a function of oxide thickness. SS is calculated from the inverse maximum slope of log10(ID) versus VG and increases from 70.57 to 91.31 mV/dec as tox increases from 1 to 5 nm

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3.4. Quantitative summary

Table 1 summarizes the extracted metrics. The trend is internally consistent: increasing t_{ox} raises both V_{th} and SS. The nearly linear behavior over the studied range suggests that oxide thickness can be used as a compact design knob in preliminary TCAD exploration. Analytical and semi-analytical models of subthreshold behavior also support the conclusion that oxide capacitance and gate electrostatics strongly influence SS and threshold shift [24, 25].

Table 1. Extracted device metrics under tox scaling

t_{ox} (nm)	V_{th} (V), $I_D = 1 \times 10^{-7}$ A	SS (mV/dec)
1	0.029	70.57
2	0.147	75.69
3	0.267	80.85
4	0.391	86.06
5	0.517	91.31

4. Conclusion

A Silvaco TCAD study was carried out to quantify the impact of gate-oxide thickness on MOSFET transfer characteristics. The oxide thickness was swept from 1 to 5 nm under a fixed drain bias of V_D = 0.05 V. The simulated transfer curves shift toward higher gate voltage as t_{ox} increases, confirming the reduction in electrostatic gate control. Using the constant-current method with $I_D = 1 \times 10^{-7}$ A, V_{th} increases from 0.029 to 0.517 V. Using the inverse maximum-slope definition, SS increases from 70.57 to 91.31 mV/dec. These results show that oxide-thickness scaling simultaneously affects threshold voltage and switching steepness. The study provides a concise TCAD-based framework for evaluating gate-stack design choices and can be extended to high-k dielectrics, interface traps, temperature dependence, and circuit-level compact-model calibration.

References

[1] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd ed. Hoboken, NJ, USA: Wiley, 2007.
[2] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 2nd ed. Cambridge, U.K.: Cambridge University Press, 2009.
[3] Silvaco, ATLAS User's Manual: Device Simulation Software. Santa Clara, CA, USA: Silvaco, 2006.
[4] Silvaco, "Semiconductor process and device simulation: TCAD software solutions, " Silvaco, 2026. [Online]. Available: silvaco.com/tcad/
[5] Silvaco, "Silvaco TCAD: Introduction and the basics—Part 2, " Silvaco Webinar, 2019. [Online]. Available: silvaco.com/webinar/
[6] IEEE International Roadmap for Devices and Systems, "2023 IRDS Metrology, " IEEE, 2023.
[7] IEEE International Roadmap for Devices and Systems, "2024 IRDS Metrology, " IEEE, 2024.
[8] G. Pananakakis, G. Ghibaudo, and S. Cristoloveanu, "Threshold voltage in FD-SOI MOSFETs, " Solid-State Electronics, vol. 217, Art. no. 108947, 2024.
[9] G. Pananakakis, G. Ghibaudo, and S. Cristoloveanu, "Detailed comparison of threshold voltage extraction methods in FD-SOI MOSFETs, " Solid-State Electronics, 2023.
[10] P. Guo et al., "Simulation of novel nano low-dimensional FETs at the scaling limit, " Nanomaterials, vol. 14, no. 17, Art. no. 1375, 2024.
[11] A. Ülkü, R. Kaçar, E. Uçar, and E. Menşur, "Reducing off-state and leakage currents by dielectric permittivity-graded stacked gate oxides on Trigate FinFETs: A TCAD study, " Micromachines, vol. 15, no. 6, Art. no. 726, 2024.

DOI: 10.54254/2753-8818/2026.34200

[12] P. Yugender, R. S. Dhar, S. Nanda, K. Kumar, P. Sakthivel, and A. Thirumurugan, "Enhanced drive current in 10 nm channel length gate-all-around field-effect transistor using ultrathin strained Si/SiGe channel, " Micromachines, vol. 15, Art. no. 1455, 2024.
[13] H. Kim and D. Lim, "Doping-less feedback field-effect transistors, " Micromachines, vol. 15, no. 3, Art. no. 316, 2024.
[14] J. S. Ko et al., "Sub-nanometer equivalent oxide thickness and threshold voltage control in MoS2 transistors, " Nano Letters, 2025.
[15] J. H. Park et al., "Enhancing InGaZnO transistor current through high-k gate dielectrics, " Scientific Reports, 2025.
[16] P. Kumar et al., "Modeling and simulation of ZnO-based thin-film transistors by dielectric engineering, " Scientific Reports, 2025.
[17] C.-E. Oh et al., "Effects of channel length on temperature dependence of apparent subthreshold swing in self-aligned top-gate coplanar IGZO thin-film transistors, " Scientific Reports, 2025.
[18] R. K. A. Bennett et al., "Mobility and threshold voltage extraction in transistors with gate-dependent contact resistance, " npj 2D Materials and Applications, 2025.
[19] R. Mosalanezhad et al., "Silvaco TCAD modeling, optical simulation, and analysis of semiconductor devices, " Scientific Reports, 2026.
[20] W. Lee et al., "TCAD simulation of STI depth and SiO2/silicon interface trap effects on MOSFET characteristics, " 2026.
[21] M. Zareiee et al., "A stepped-spacer FinFET design for enhanced device performance, " Micromachines, 2025.
[22] M. Li et al., "A TCAD simulation-based study of FinFETs and GAAFETs for short-channel-effect suppression, " 2025.
[23] A. Tariq et al., "Pre-silicon accurate SPICE modeling of trench MOSFETs based on TCAD simulations, " Micromachines, vol. 16, no. 8, Art. no. 955, 2025.
[24] J. Talukdar et al., "Analytical modeling and TCAD simulation for subthreshold characteristics of asymmetric tunnel FETs, " Superlattices and Microstructures, 2022.
[25] P. Banerjee et al., "Threshold-voltage modeling-based comparative exploration of high-k gate-stack cylindrical gate-all-around MOSFETs, " Materials Science in Semiconductor Processing, 2024.